P03

Electromagnetic Design of Integrated CMOS Frequency Multiplier Chains for Sub-THz Frontend Architectures

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The realization of compact signal generation circuits above 100 GHz remains one of the key technological challenges limiting the broader deployment of sub-terahertz systems for communication, sensing, imaging, and radar applications [1]. While III-V and SiGe technologies dominate high-performance implementations, CMOS provides a scalable and cost-effective platform for compact sub-THz frontend integration [2]. However, efficient frequency multiplication in standard CMOS technologies becomes increasingly challenging due to passive losses, parasitic coupling, impedance matching constraints, and limited transistor performance at elevated frequencies.

This work presents the design and electromagnetic modeling of integrated frequency multiplier chains implemented in a 65 nm CMOS technology for sub-THz applications. The investigated architectures include a Ka-to-W-band frequency tripler and a subsequent multiplication stage targeting D-band as well as operation in the 220-300 GHz frequency range. In contrast to studies focused solely on multiplier cores, the proposed approach considers the complete frontend circuitry, including integrated amplification stages intended to compensate conversion losses between multiplication stages, together with baluns, matching networks, filtering structures, transmission lines, and antenna interfaces. The complete multiplier-chain frontend occupies only 1 × 0.5 mm², including RF pads.

At sub-THz frequencies, circuit performance is strongly influenced by electromagnetic coupling and parasitic effects from integrated passive structures. Therefore, particular attention was devoted to the co-design and optimization of passive components and their interaction with active multiplier cores. Full-wave electromagnetic and circuit-level co-simulations were used to evaluate harmonic generation, impedance matching, signal propagation, and passive loss effects on frontend performance.

Simulation results demonstrate the feasibility of integrated CMOS-based multiplier chains operating toward the sub-THz frequency range while maintaining compact implementation and suitable signal propagation characteristics. The presented study highlights the importance of accurate passive component co-design for efficient operation above 100 GHz and provides insight into practical challenges associated with highly integrated CMOS sub-THz frontend realization.

REFERENCES

[1] G. Wang et al.; *Terahertz integrated sensing and mobile communications empowered by a 220-GHz-band portable device*, Nature Communications, 16 (2025), 11719.

[2] R. Chen, B. Yan and M. F. Chang; *A Review of Circuits and Systems for Advanced Sub-THz Transceivers in Wireless Communication*, MDPI Electronics, 14 (2025), 861.